

# INTERNATIONAL STANDARD



**Semiconductor devices – Flexible and stretchable semiconductor devices –  
Part 9: Performance testing methods of one transistor and one resistor (1T1R)  
resistive memory cells**



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INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

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**SEMICONDUCTOR DEVICES – FLEXIBLE AND  
STRETCHABLE SEMICONDUCTOR DEVICES –**
**Part 9: Performance testing methods of one transistor  
and one resistor (1T1R) resistive memory cells**
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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at [www.iec.ch/members\\_experts/refdocs](http://www.iec.ch/members_experts/refdocs). The main document types developed by IEC are described in greater detail at [www.iec.ch/standardsdev/publications](http://www.iec.ch/standardsdev/publications).

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# SEMICONDUCTOR DEVICES – FLEXIBLE AND STRETCHABLE SEMICONDUCTOR DEVICES –

## Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells

### 1 Scope

This part of IEC 62951 specifies the test methods for evaluating the performance of unipolar-type one transistor one resistor (1T1R) resistive memory cells. The performance test methods in this document include read, forming, SET, RESET, endurance and retention. This document is applicable to flexible devices as well as rigid resistive memory devices without any limitations prone to device technology and size.

### 2 Normative references

There are no normative references in this document.

### 3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

#### 3.1

##### **programming transistor**

semiconductor device used to amplify, limit or switch electronic signals and electrical power

#### 3.2

##### **source voltage**

$V_S$

bias applied to the source terminal of the programming transistor

#### 3.3

##### **gate voltage**

$V_G$

bias applied to the gate terminal of the programming transistor

#### 3.4

##### **drain voltage**

$V_D$

bias applied to the drain terminal of the programming transistor

#### 3.5

##### **resistive memory**

two terminal device, based on reversible formation and rupture of filament within active layer, defining low and high resistance states, respectively